Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2-20. (Previously Canceled)

21. (New) A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which stores n bits data (3 <n, n being an integer);

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

a plurality of data storage circuits which are connected to said plurality of bit lines in a one-to-one correspondence;

a first latch circuit included in each of the data storage circuits, which store one of the input data and the output data;

a second latch circuit included in each of the data storage circuits;

a write circuit, which writes the input data stored in one of the first latch circuit to the memory cells; and

a write verify circuit which verifies the data of the memory cells, the data verified by the write verify circuit is stored in another latch circuit of the second latch circuit.

22. (New) The device according to claim 21, wherein said plurality of memory cells arranged in a matrix are nonvolatile memory cells.

23. (New) The device according to claim 21, wherein said plurality of memory cells arranged in the column direction are connected in series.

24. (New) The device according to claim 21, wherein said plurality of memory cells arranged in the column direction are connected in series to configure a NAND cell.

25. (New) The device according to claim 21, wherein the first latch circuit is inserted between a data input/output buffer circuit and one of the bit lines.

26. (New) The device according to claim 21, further comprising a transistor inserted between the first latch circuit and the input/output buffer circuit.

27. (New) The device according to claim 21, further comprising a first clocked inverter circuit connected parallel to the transistor.

28. (New) The device according to claim 21, wherein the second latch circuit is connected to one of the bit lines.

29. (New) The device according to claim 23, wherein the first latch circuit is configured by second and third clocked inverter circuits.

30. (New) The device according to claim 26, wherein the second latch circuit is configured by fourth and fifth clocked inverter circuits.

31. (New) The device according to claim 25, wherein said plurality of memory cells arranged in a matrix are nonvolatile memory cells.

32. (New) The device according to claim 25, wherein said plurality of memory cells arranged in the column direction are connected in series.

33. (New) The device according to claim 25, wherein said plurality of memory cells arranged in the column direction are connected in series to configure a NAND cell.